Amendments to the Specification

Please amend the specification of the application as follows:

Please replace the paragraph beginning on page 9 line 10 with the following paragraph as amended:

Various embodiments of the present invention will now be described with reference to a number of drawings. The various embodiments may include one or more buffers (e.g., jitter buffers) that can store data from multiple data channels, as well as a corresponding valid data memory (e.g., a jitter buffer state valid bit (JBVB) memory) that can provide a rapid and/or convenient indication of the state of buffered voice data for the multiple voice channels.

Please replace the paragraph beginning on page 14 line 21 with the following paragraph as amended:

While JBVB memories (**302**-0 to **302**-3) may be formed from a device that is independently accessible with respect to jitter buffers (**300**-0 to **300**-3), JBVB memories (**302**-0 to **302**-3) may ~~have~~ be formed in a common address space. By example, base addresses for various JBVB memories **302**-0 to **302**-3 in FIG. 3 are shown as BASE 16JBVB, BASE 32JBVB, BASE 64JBVB, and BASE 128JBVB, respectively. As will be described in more detail herein, the same address that accesses data in a jitter buffer (**300**-0 to **300**-3) may be used to access corresponding bit(s) in a JBVB memory (**302**-0 to **302**-3) by "swizzling" the jitter buffer address. Such an arrangement, may improve the speed at which a JBVB memory (**302**-0 to **302**-3) may be updated as a corresponding jitter buffer memory (**300**-0 to **300**-3) is accessed.

Please replace the paragraph beginning on page 18 line 23 with the following paragraph as amended:

Referring now to FIG. ~~4B~~ 6B, like the previous examples, a JBVB memory **602** may arrange the various channels of a corresponding jitter buffer into groups. Again, because it may be convenient when multiple JBVB memories are stored in the same memory device, each group can includes 32 channels. However, unlike the previous examples, and as illustrated in FIG. ~~4B~~ 6B, each JBVB memory entry may provide the status for two dwords

of a jitter buffer. Thus, each group of JBVB memory **602** can include 128 entries that correspond to the 256 dwords for given voice channels.

Please replace the paragraph beginning on page 19 line 17 with the following paragraph as amended:

FIG. 7 shows a table that illustrates how a JBVB memory address may be generated. A column "BUFFER SIZE" indicates how the generation of a JBVB memory address can vary according to which particular jitter buffer is accessed. Four possible jitter buffers are shown in FIG. ~~6~~ 7: a 16 ms, 32 ms, 64 ms, and 128 ms buffer. In the case of a 16 ms buffer access, a corresponding JBVB memory may include multiple portions of a jitter buffer address (bits [16:12] and bits[6:2]). This value can be added to a base address for a 16 ms JBVB memory (BASE 16JBVB). Finally, as will be recalled, in the particular jitter buffer address arrangement of FIG. 4A, each channel could have a particular dword selectable from among 32 dwords. A jitter buffer address could include bits [11:7] for selecting a particular dword. These same bits can be utilized to generate a bit mask for data read from a JBVB memory entry. The generation of bit masks is well understood in the art, and so will not be described in detail herein.

Please replace the paragraph beginning on page 27 line 3 with the following paragraph as amended:

FIG. 11B shows a subsequent read for CH3 from a jitter buffer to a local buffer **1104**. However, unlike the case of FIG. 11A, corresponding JBVB data is invalid. In the example of FIG. 11B, entry ~~**1112**~~ **1110** may now be considered a "previous" local buffer entry, while entry **1110'** is now a current local buffer entry. A local buffer address accesses both entries (~~**1112**~~ **1110** and **1110'**). However, because JBVB data is not valid, jitter buffer data is not output by a multiplexer **1108**. Instead, multiplexer **1108** can provide data from a replicator **1106** as an output.